Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Please cancel claims 1-7, 9-11, 13-19, 22, and 28-30 without prejudice and amend claim 12 as follows:

1-11 (canceled)

12. (currently amended) The processor of claim ~~4~~ 39 wherein the adaptable pipeline control unit further comprises:

a programmable clock gating mode indicator that specifies a normal clock gating mode and a slow down clock gating mode; and

control for extending pipeline stage timing for both first class ~~1~~ instructions and second class ~~2~~ instructions to execute in a longer time period than required to execute the second class instructions ~~execution latency~~ when the programmable clock gating mode indicator specifies a slow down clock gating mode.

13-30 (canceled)

31. (new) A processor with an instruction class controllable pipeline comprising:

an adaptable decode stage that decodes in a first time period an instruction received from an instruction register, stores the decoded instruction in a decode register, and generates an

instruction class indication that identifies the decoded instruction as a first class instruction or as a second class instruction;

an adaptable execution stage that executes an identified first class instruction in a first class execution logic circuit or executes an identified second class instruction in a second class execution logic circuit in response to the instruction class indication, wherein the first class execution logic circuit has a worst-case signal propagation time that is less than or equal to a first class time period and the second class execution logic circuit has a worst-case signal propagation time that is greater than the first class time period and assigned to a second class time period; and

an adaptable pipeline control unit responsive to the instruction class indication for an identified second class instruction to select the second class execution logic circuit and to hold the decoded instruction in the decode register until the first time period plus a second time period is equal to the second class time period, wherein stages of the class controllable pipeline advance at a rate that allows the identified second class instruction to complete operations in the adaptable execution stage.

32. (new) The processor of claim 31, wherein the adaptable pipeline control unit selects the first class execution logic circuit in response to the instruction class indication for an identified first class instruction, wherein stages of the class controllable pipeline advance at a rate that allows the identified first class instruction to complete operations in the adaptable execution stage.

33. (new) The processor of claim 31 further comprises:

an adaptable fetch stage for fetching the instruction in the first time period to the instruction register, wherein the adaptable pipeline control unit holds the instruction in the instruction register the second time period until the first time period plus the second time period is equal to the second class time period.

34. (new) The processor of claim 33, wherein the adaptable pipeline control unit comprises:

a program counter; and

a program counter update function, wherein the adaptable pipeline control unit in response to the instruction class indication for an identified second class instruction holds program counter state and prevent a fetch operation until a hold pipeline signal is released.

35. The processor of claim 31, wherein the adaptable decode stage comprises:

a decode register feedback multiplexer having a first input coupled to an output of a decode function, a second input coupled to an output of the decode register, a select input, and an output coupled to an input of the decode register, wherein the decode register feedback multiplexer selects the output of the decode register to be coupled to the input of the decode register in response to a hold signal to hold the contents of the decode register for the period of the hold signal.

36. (new) The processor of claim 31, wherein an independent first class instruction enters execution in the first class execution logic circuit while an independent second class instruction enters a second half of execution in the second class execution logic circuit, wherein both the first class instruction and the second class instruction complete operations on their respective execution logic circuit by the end of the second class time period.

37. (new) The processor of claim 31, wherein the instruction is defined as a first class instruction based on an encoding of the instruction that specifies either a byte or a half-word operation.

38. (new) The processor of claim 31, wherein the instruction is defined as a second class instruction based on an encoding of the instruction that specifies either a word or a double-word operation.

39. (new) A processor with an instruction class controllable pipeline comprising:

an adaptable decode stage that decodes an instruction received from an instruction register, stores the decoded instruction in a decode register, and generates an instruction class indication that identifies the decoded instruction as a first class instruction or as a second class instruction;

an adaptable execution stage that executes an identified first class instruction in a first class execution logic circuit or executes an identified second class instruction in a second class execution logic circuit in response to the instruction class indication, wherein the first class execution logic circuit has a worst-case signal propagation time that is less than or equal to a first

class time period and the second class execution logic circuit has a worst-case signal propagation time that is greater than the first class time period; and

an adaptable pipeline control unit responsive to the instruction class indication for an identified second class instruction to select the second class execution logic circuit and to adjust a period of an adaptable period pipeline clock to allow time for the identified second class instruction to complete operations in the adaptable execution stage.

40. (new) The processor of claim 39, wherein the first class time period corresponds to a first multiple of cycles of a master clock and the second class execution logic circuit's worst-case signal propagation time corresponds to a second multiple of cycles of the master clock and wherein the period of the adaptable period pipeline clock is adjusted according to the second multiple of cycles of the master clock.

41. (new) The processor of claim 40, wherein the adaptable pipeline control unit in response to the instruction class indication for an identified first class instruction selects the first class execution logic circuit and adjusts the period of the adaptable period pipeline clock according to the first multiple of cycles of the master clock to allow time for the identified first class instruction to complete operations in the adaptable execution stage.

42. (new) The processor of claim 39 further comprises:

an adaptable fetch stage for fetching the instruction to the instruction register, wherein the adaptable period pipeline clock clocks the adaptable fetch stage.

43. (new) The processor of claim 39, wherein the instruction is defined as a first class instruction based on a first encoding of the instruction that specifies a first number of cycles of a master clock to adjust the period of the adaptable period pipeline clock to a first period.

44. (new) The processor of claim 43, wherein the first class instruction is encoded as a second class instruction using a different encoding of the instruction than the first encoding and wherein the different encoding specifies a second number of cycles of the master clock to adjust the period of the adaptable pipeline clock to a second period longer than the first period to minimize power.

45. (new) The processor of claim 43, wherein the instruction is defined as a second class instruction based on an encoding of the instruction that specifies a second number of cycles of a master clock to adjust the period of the adaptable period pipeline clock to a second period, wherein the second period is longer than the first period.

46. (new) The processor of claim 39, wherein the adaptable period pipeline clock is a logic gated version of the master clock, wherein the clock gating logic is responsive to the instruction class indication.

47. (new) A processor with an instruction class controllable pipeline comprising:

an adaptable decode stage that decodes an instruction received from an instruction register, stores the decoded instruction in a decode register, and generates an instruction class indication that identifies the decoded instruction as a first class instruction or as a second class instruction;

an adaptable execution stage that executes an identified first class instruction in a first class execution logic circuit or executes an identified second class instruction in a second class execution logic circuit in response to the instruction class indication, wherein the first class execution logic circuit has a worst-case signal propagation time that is less than or equal to a first class time period and the second class execution logic circuit has a worst-case signal propagation time that is greater than the first class time period and assigned to a second class time period; and

an adaptable pipeline control unit responsive to the instruction class indication for an identified second class instruction to select the second class execution logic circuit and to adjust a period of an adaptable period pipeline clock to allow time for the identified second class instruction to complete operations in the adaptable execution stage, wherein the adaptable execution stage is synthesized by a single pass synthesis methodology with the period of the adaptable period pipeline clock set to the second class time period during synthesis.

48. (new) The processor of claim 47, wherein the first class execution logic circuit comprises:

a first class combinatorial logic circuit that receives the decoded instruction from the decode register to execute a first class logic function associated with the identified first class instruction and generates a first class output; and

a first class non-inverting buffer circuit receives the first class output, delays the first class output for a two class processor architecture by a first class delay that is equal to a difference between the second class time period and the first class time period.

49. (new) The processor of claim 47, wherein the second class execution logic circuit comprises:

a second class combinatorial logic circuit that receives the decoded instruction from the decode register to execute a second class logic function associated with the identified second class instruction and generates a second class output; and

a second class non-inverting buffer circuit receives the second class output, delays the second class output for a two class processor architecture by a minimum propagation delay associated with a non-inverting buffer available in a hardware description language (HDL) library of standard cells.